

LH532600

CMOS 2M (256K × 8/128K × 16)
Mask-Programmable ROM

FEATURES

- 262,144 words × 8 bit organization (Byte mode)
131,072 words × 16 bit organization (Word mode)
- Access time: 100 ns (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Power consumption:
Operating: 412.5 mW (MAX.)
Standby: 550 μW (MAX.)
- Mask-programmable control pin:
Pin 1 = OE₁/ $\overline{\text{OE}}_1$ /DC
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP
48-pin, 10 × 20 mm² TSOP (Type I)

DESCRIPTION

The LH532600 is a 2M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by BYTE input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

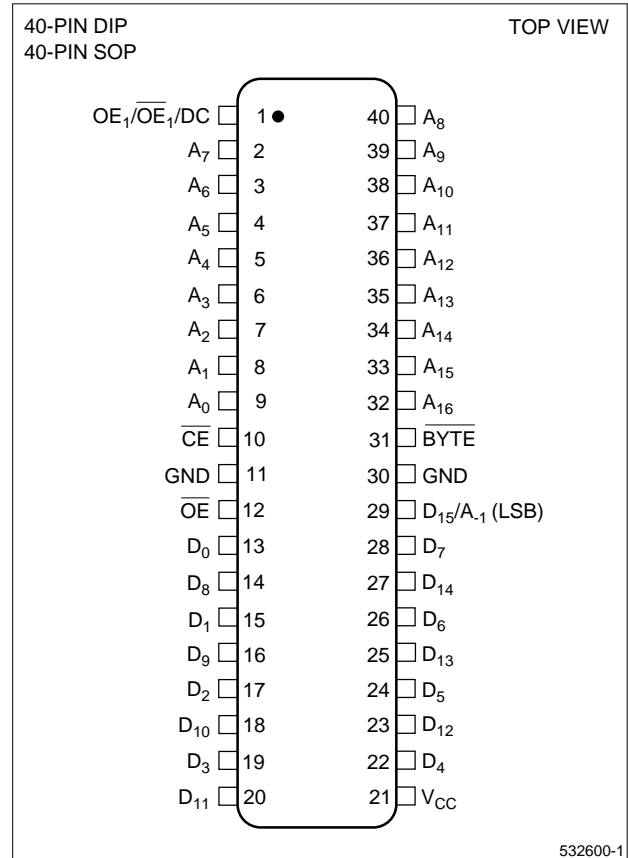


Figure 1. Pin Connections for DIP and SOP Packages

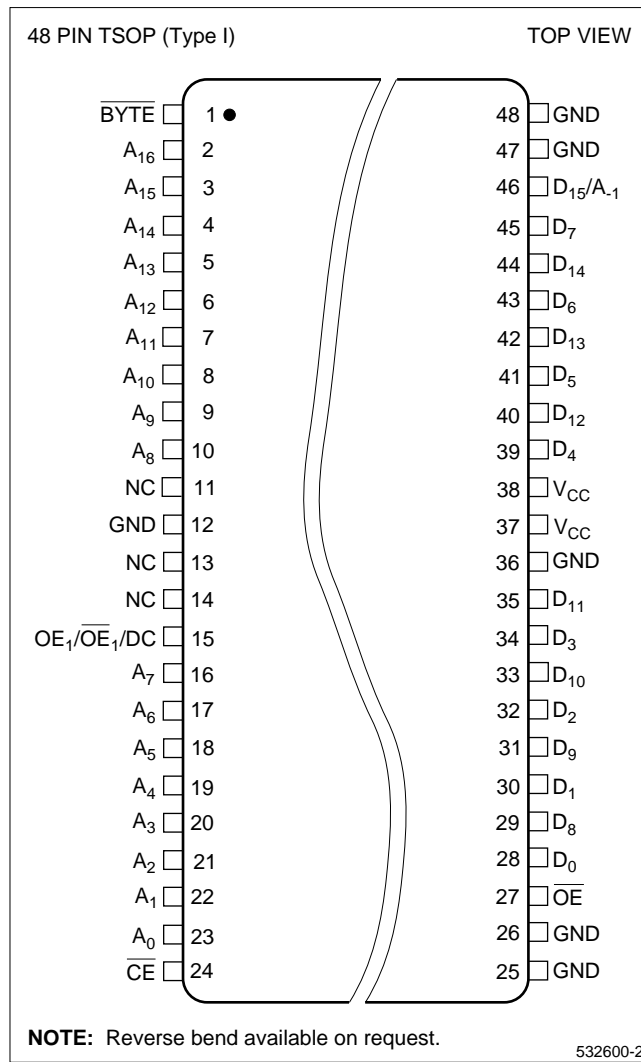


Figure 2. Pin Connections for TSOP Package

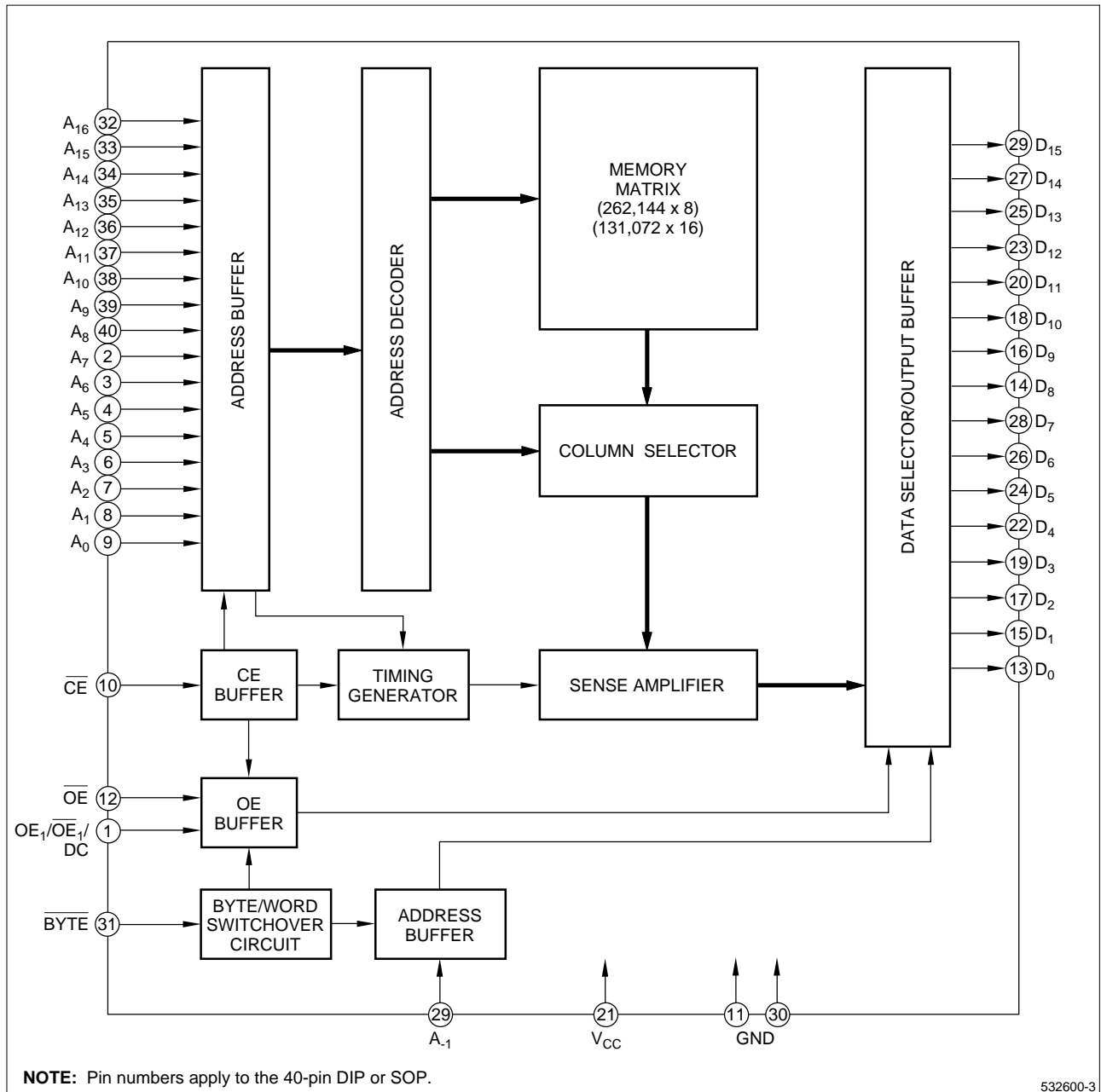


Figure 3. LH532600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₁ – A ₁₆	Address input	1
D ₀ – D ₁₅	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
\overline{OE}	Output enable input	
OE ₁ / \overline{OE} ₁ /DC	Output enable input	2, 3
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. The D₁₅/A₁ pin becomes LSB address input (A₁) when the \overline{BYTE} pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.
2. Active levels of OE₁/ \overline{OE} ₁/DC are mask-programmable. When DC is selected out of OE₁/ \overline{OE} ₁/DC, it is fixed to an active level. Then it is recommended to apply either V_{IH} or V_{IL} to the DC pin.
3. DC = Don't care.

TRUTH TABLE

\overline{CE}	\overline{OE}	OE_1/\overline{OE}_1	BYTE	A ₋₁ (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					D ₀ – D ₇	D ₈ – D ₁₅	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby
L	H	X	X	X	High-Z	High-Z	–	–	Operating
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating
L	L	H/L	H	–	D ₀ – D ₇	D ₈ – D ₁₅	A ₀	A ₁₆	Operating
L	L	H/L	L	L	D ₀ – D ₇	High-Z	A ₋₁	A ₁₆	Operating
L	L	H/L	L	H	D ₈ – D ₁₅	High-Z	A ₋₁	A ₁₆	Operating

NOTE:

X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}		2.2	V _{CC} + 0.3	V	
Input 'Low' voltage	V _{IL}		–0.3	0.8	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4		V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 100 ns		75	mA	2
	I _{CC2}	t _{RC} = 1 μs		65	mA	2
	I _{CC3}	t _{RC} = 100 ns		70	mA	3
	I _{CC4}	t _{RC} = 1 μs		60	mA	3
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$		100	μA	
Input capacitance	C _{IN}	f = 1 MHz		10	pF	
Output capacitance	C _{OUT}	T _A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE}/\overline{OE}_1 = V_{IH}$, $OE_1 = V_{IL}$
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
Chip enable access time	t_{ACE}		100	ns	
Output enable delay time	t_{OE}		55	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		55	ns	1
OE to output in High-Z	t_{OHZ}				

NOTE:

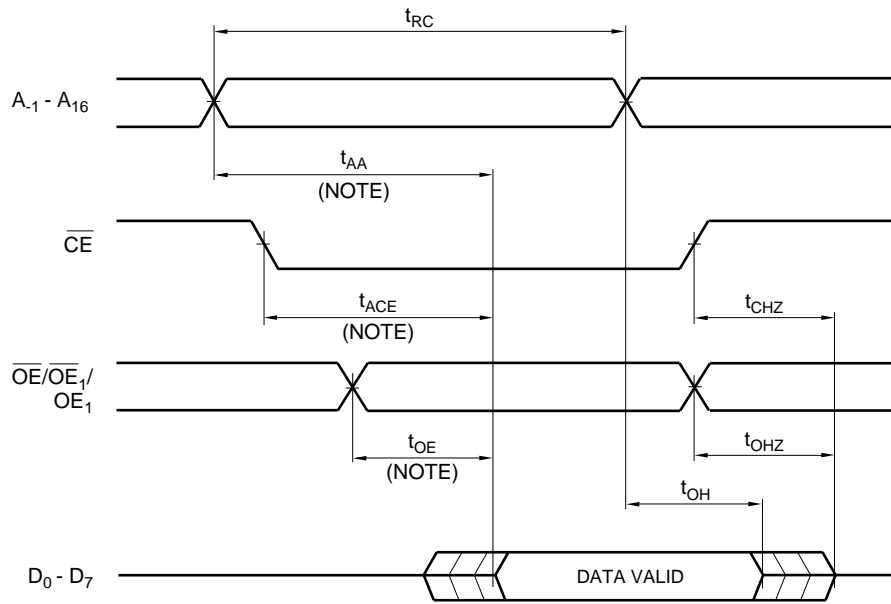
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

CAUTION

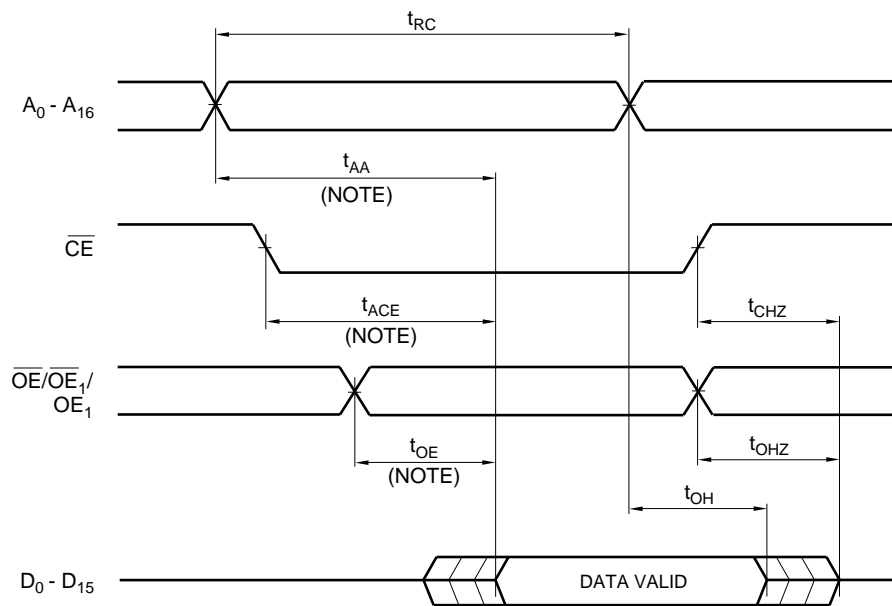
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last intervals, t_{AA} , t_{ACE} , or t_{OE} , have concluded.

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Figure 4. Byte Mode ($\overline{BYTE} = V_{IL}$)

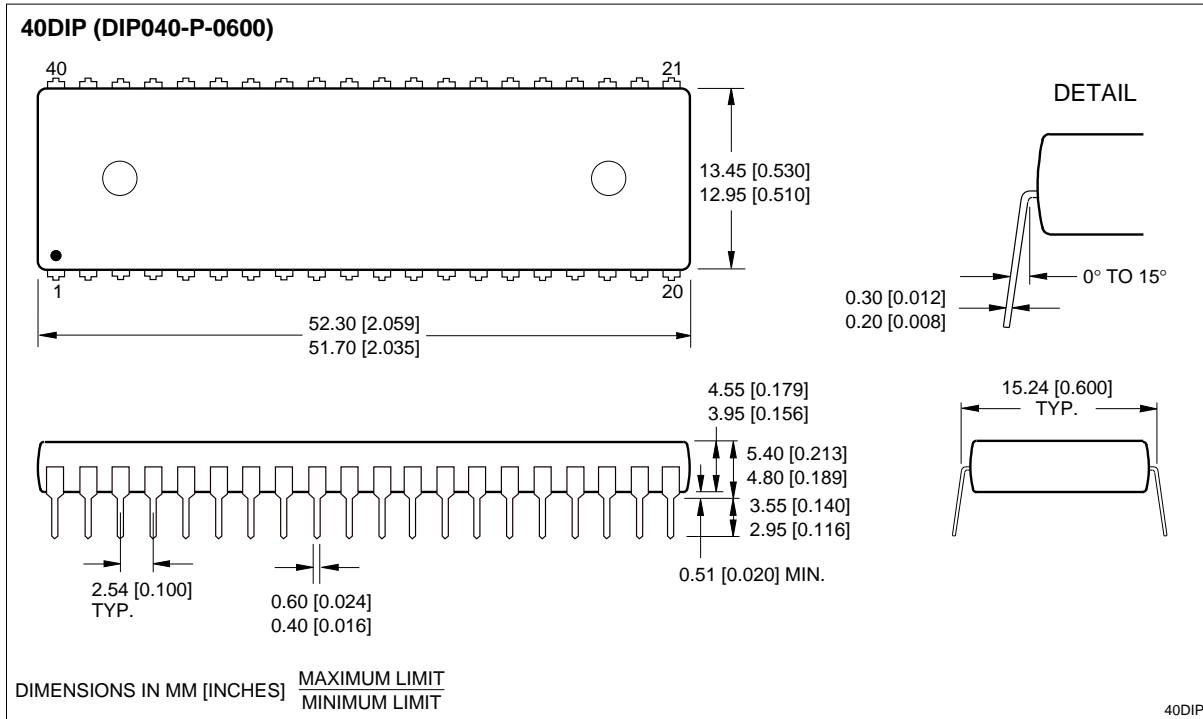


NOTE: The output data becomes valid when the last intervals, t_{AA} , t_{ACE} , or t_{OE} , have concluded.

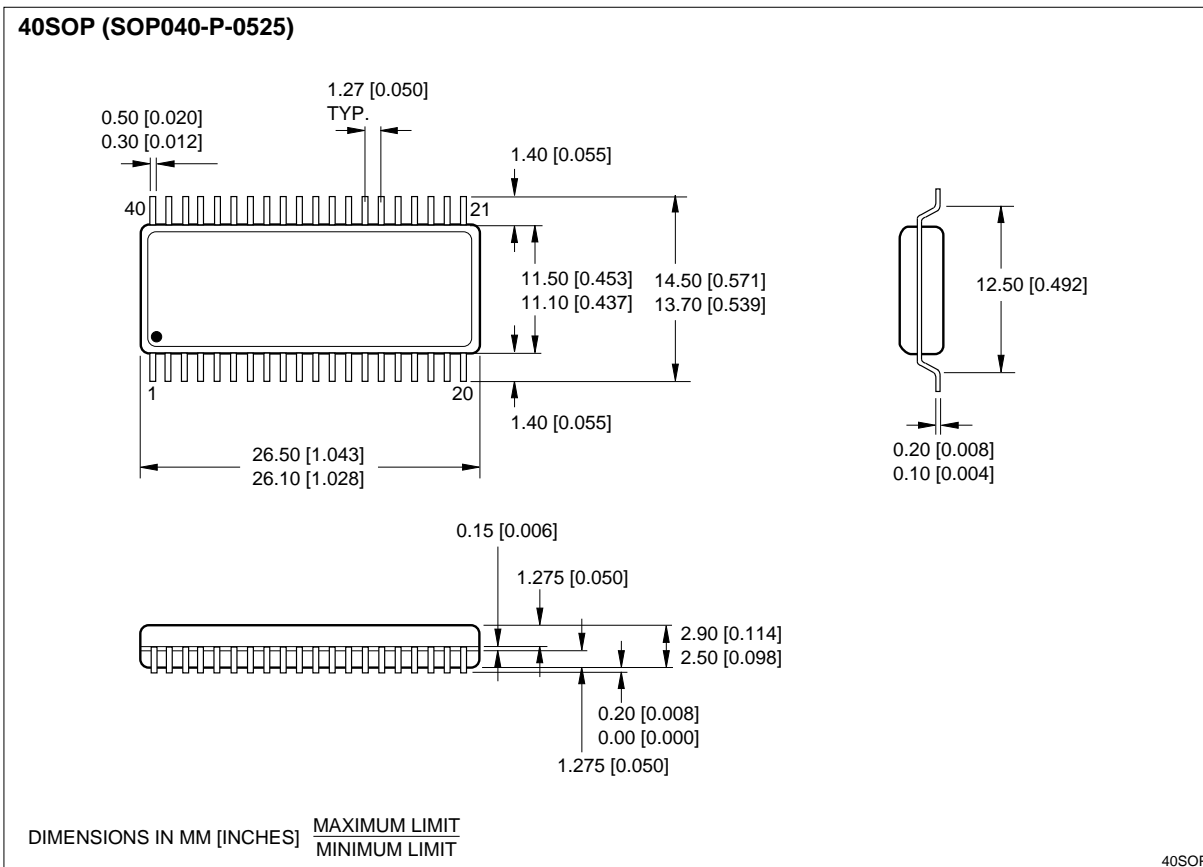
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Figure 5. Word Mode ($\overline{BYTE} = V_{IH}$)

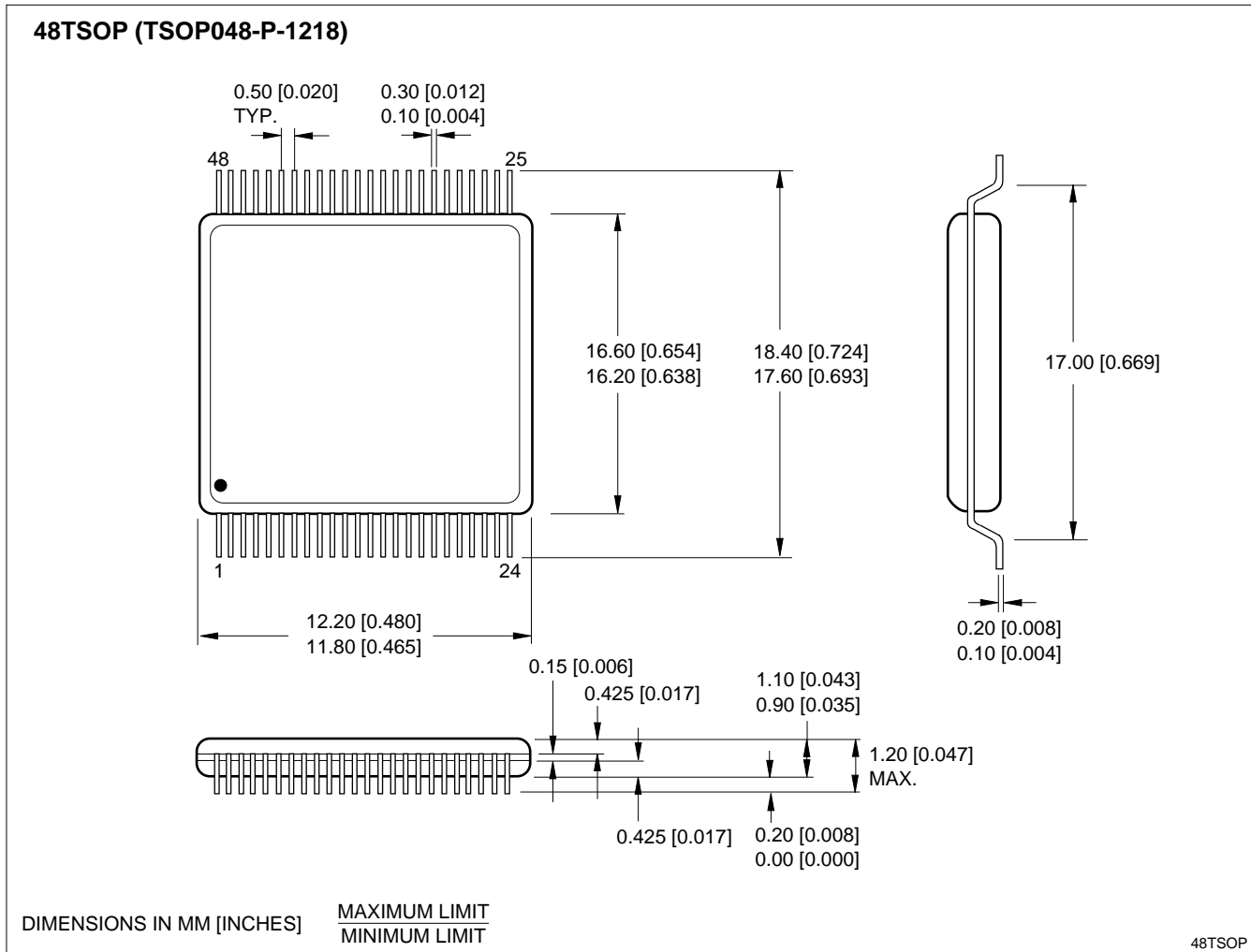
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP



48-pin, 10 × 20 mm² TSOP (Type I)

ORDERING INFORMATION

